

```

graph LR
    102[HOST] <--> 120[INTERFACE]
    120 <--> 118[DATA BUFFER]
    118 <--> 116[ECC]
    116 <--> 114[ENDEC]
    114 <--> 112[CHANNEL]
    112 <--> 106[TRANSUCER]
    106 <--> 104[DISK]
    112 <--> 122[SERVO]
    122 <--> 108[ACTUATOR ASSEMBLY]
    108 <--> 110[VCM]
    124[DISK CONTROLLER/MICROPROCESSOR] <--> 120
    124 <--> 118
    124 <--> 116
    124 <--> 114
    124 <--> 112
    124 <--> 122
  
```

FIG. 1

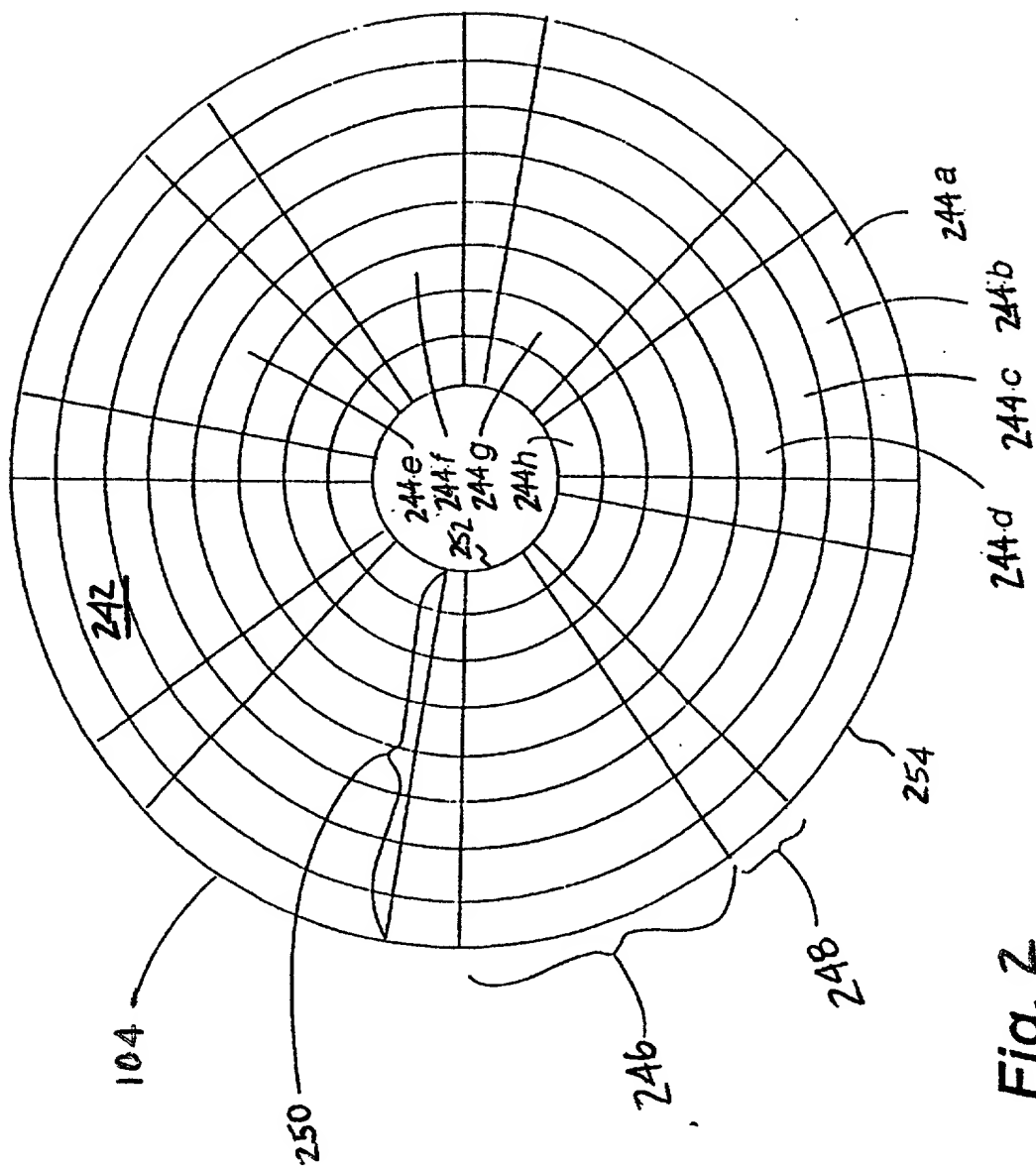


Fig. 2

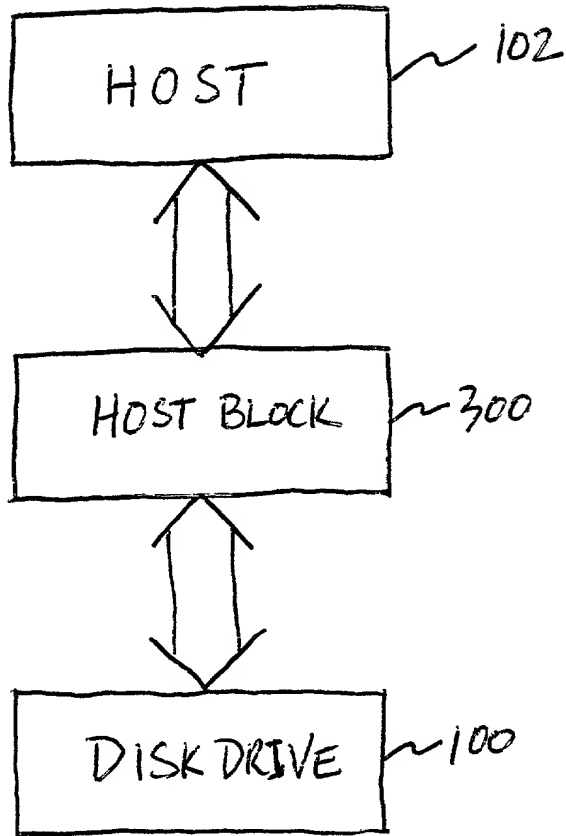


FIGURE 3

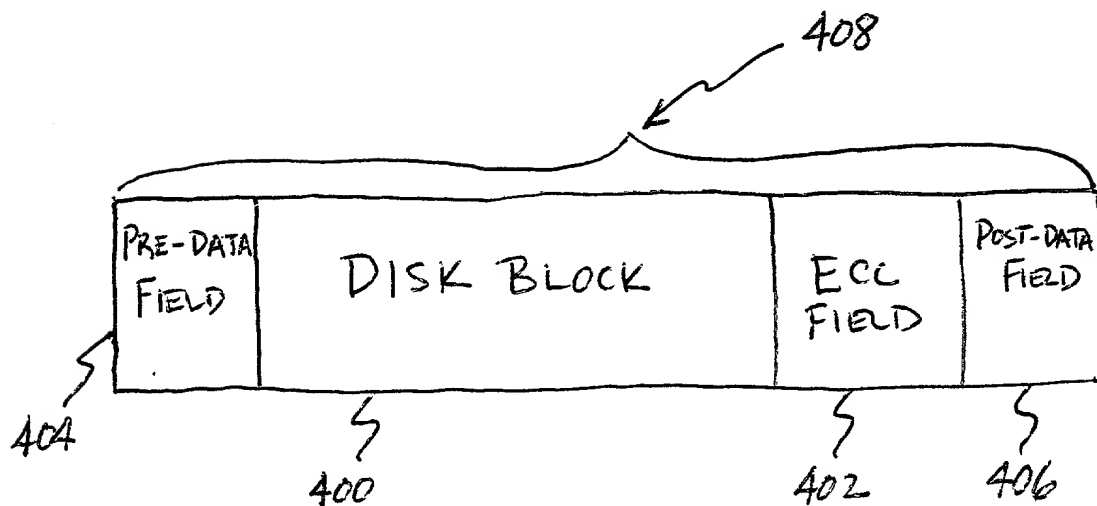


FIGURE 4

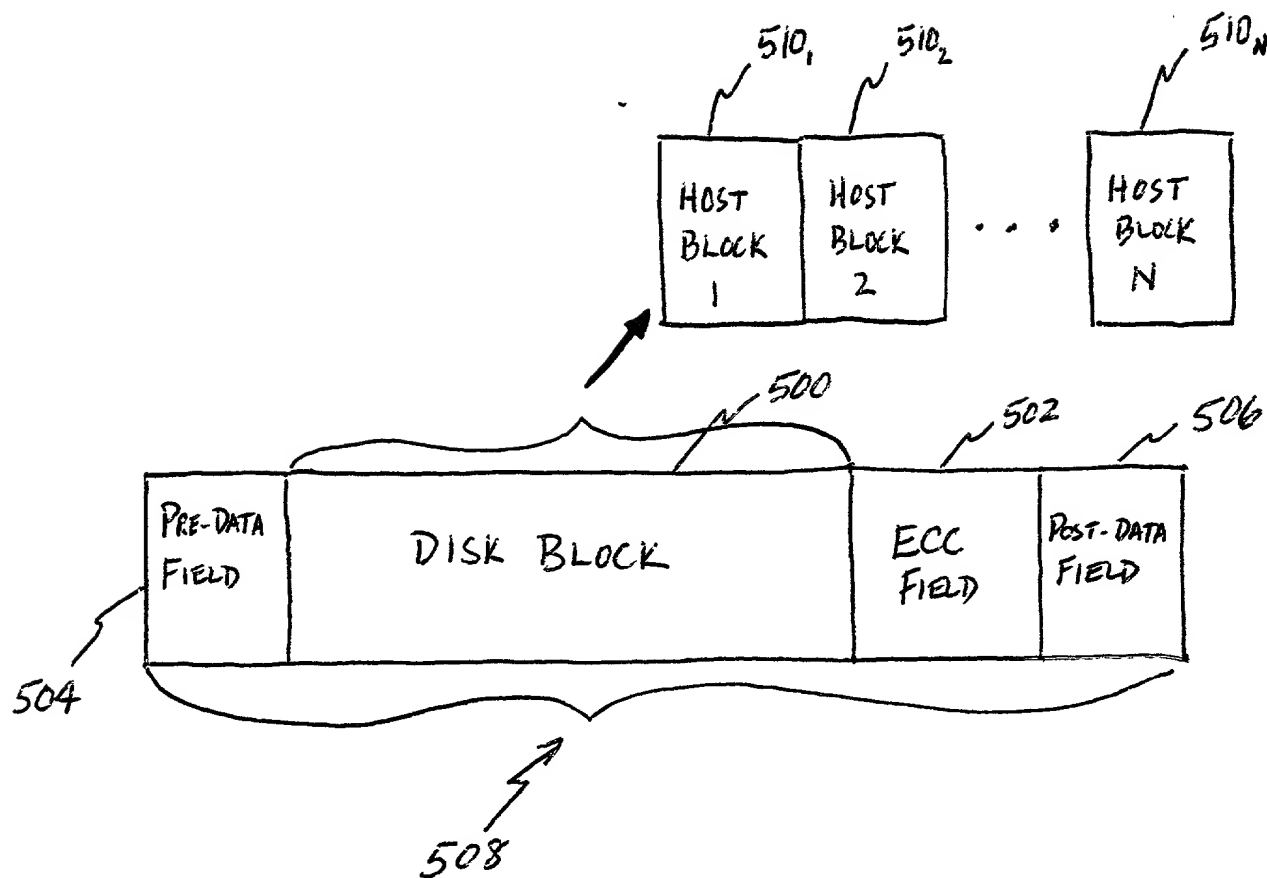


FIGURE 5

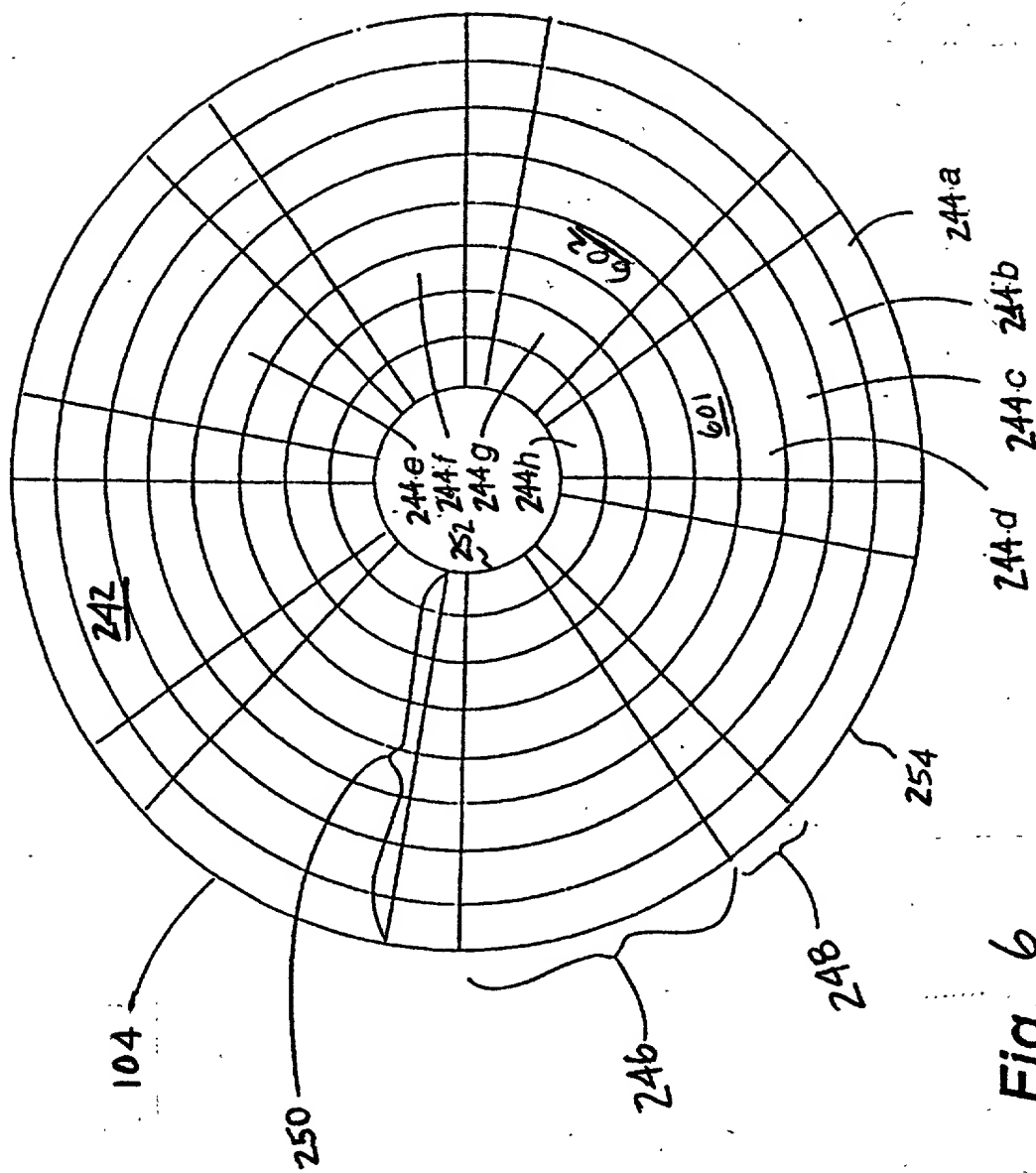


Fig. 6

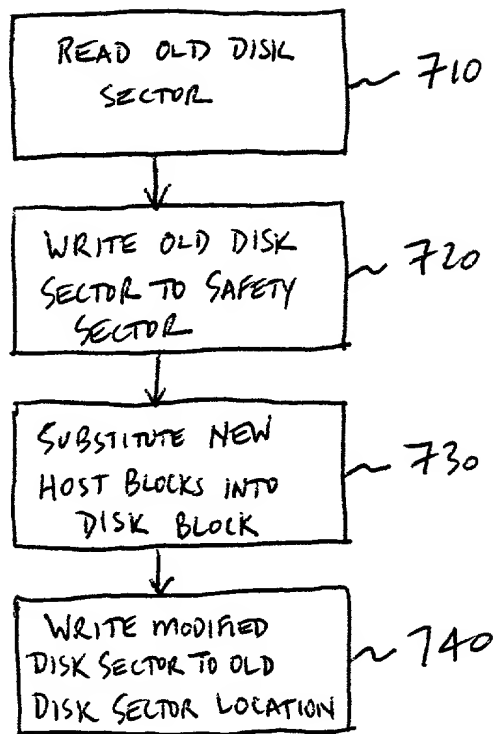


FIGURE 7